REMARKS

Claims 1 to 8 are pending. Claims 1 to 8 are currently rejected. Claims 1 and 4 are currently amended. Reconsideration of the application is requested.

§ 103 Rejections

Applicants respectfully submit that according to MPEP 2142, to establish a case of *prima facie* obviousness, three basic criteria must be met: 1) there must be some suggestion or motivation, either in the references or generally known to one skilled in the art, to modify or combine reference teachings, 2) there must be reasonable expectation of success, and 3) the prior art references must teach or suggest all the claim limitations. The ability to modify the method of the references is not sufficient. The reference(s) must provide a motivation or reason for making the changes. *Ex parte Chicago Rawhide Manufacturing Co., 226 USPQ 438 (PTO Bd. App. 1984).*

Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregor et al. (U. S. Pat. No. 5,354,955) in view of Hanson et al. (U. S. Pat. No. 4,496,793).

The Office Action essentially states:

> Regarding claim 1, Gregor et al. discloses in e.g., Fig. 1 a laminated flip-chip interconnect package (the package in Fig. 1) comprising
> - a substrate (12; column 3, line 7) having a chip attach surface (the top surface of the substrate 12 where the chip 14 is attached) and an opposing board attach surface (the bottom surface of the substrate 12) that define contact pads (the pads under the solder ball 20 and pads on the top surface of the substrate 12) for attachment to corresponding pads on the chip (14; column 3, line 8) and board (10; column 3, line 5),
> - wherein the board attach surface (at the bottom surface of the substrate 12) comprises
>   - a pattern of contact pads (the pads under the solder ball 20) opposite and "adjacent" a chip attach location (the area on the substrate 12 where the chip 14 is attached) on the chip attach surface except at least one unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) of the board attach surface (see e.g., Fig. I),
>   - said unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) being "adjacent" to a corner of chip attach location (see e.g., Fig. l), and
> - said board attach surface (the surface that has the elements 120) comprising a dielectric material (the lowermost dielectric layer in the element 12). As shown ine.g., Fig. 1 of Gregor et al., the unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) has at least the size of a region. Gregor et al. doesn't explicitly state that the unpatterned solid plane area is at least the size at which the strain is less then the cracking strain in the thermal cycling from 125°C to -55OC. The stresses are related to the types of materials and other parameters i.e., the die size and thickness, substrate thickness, etc.

(see page 12, lines 27 - 30 of the specification of instant invention), so in a device where a crack does not occur, it can be assumed that the size is greaterthan the size at which the strain causes a crack, as if it weren't then the crack wouldoccur.

Mils SPEC Std 202 specifies that devices should operate without failures in solder joints from -55°C to +12S0C. Therefore, one of ordinary skill would have found reason, motivation and suggestion to select the material so that no cracking occurs in cycling over the operating range of -55°C to +125OC. In designing a device to exceed the standard for Mil standard 202, the lack of cracking would inherently require the absence of cracking, which would mean for the size of the unpatterned area was large enough that no cracking occurs. Furthermore, it is a common knowledge that reducing thermal stress or thermal mismatch prevents cracking in the substrate (see column 7, line 66 - column 8, line 6 of Arai et al.).

To withstand common standard thermal stress cycles, the multi-layer board must withstand more than 400 thermal stress cycles to meet Mil Std202. Inherently, any multi-layer board withstood the more than 400 thermal stress cycles per Mil Std 202which is thermal cycling of assembled circuits between-55°C to +125°C with no failures in solder joins. Thus, the unpatterned solid plane area (at the solid and nonpad areas on the back surface of the element 12 which are directly opposite areas ofthe element 25) of Gregor et al. would withstand the common standard thermal stresscycles.

Alternatively, not relying of Gregor et al.'s disclosure that the limitation "the unpatterned solid plane area being at least the size of a region in which strain due to thermal cycling from125°C to -55°C is greater than the strain at which cracking will occur in the absence of theunpatterned solid plane area" is taught by Hanson et al. in e.g., column 4, lines 54- 65 an entire area of a circuit board withstanding more than strain due to thermal cycling from 125°C to-55°C without cracking or failures. It would have been obvious to one of ordinary skill in the artat the time when the invention was made to apply the circuit board that withstands more thanstrain due to thermal cycling from 125°C to -55°C without cracking or failures of Hanson et al.to be the substrate of Gregor et al. as taught by Hanson et al. to produce an average thermal coefficient of expansion of approximately 8.9 * 10^{-6} inch per inch per degree Celsius (column 4, lines 57 - 60).

Regarding claim 4, Gregor et al. discloses in e.g., Fig. 1 a laminated flip-chip interconnect package (the package in Fig. 1) comprising

- a substrate (1 2) having a chip attach surface (the top surface of the substrate 12 where the chip 14 is attached) and an opposing board attach surface (the bottom surface ofthe substrate 12) that defines a pattern of contact pads (the pads between the solder ball 20 and the substrate 12) for attachment to corresponding pads on the chip (14)and board (10),
- wherein the board attach surface (at the bottom surface of the substrate 12) comprises
  - at least one unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of theelement 25),
  - said unpatterned area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) being opposite a chip attach surface region adjacent at least one comer of a chip attach location (see e.g., Fig. 1), and
- said board attach surface comprising a metal (At the year 1994, all wirings or circuitsor pads materials includes metal materials, i.e., copper or aluminum, etc. Thus, Gregor et al. meets this limitation.). As shown in e.g.;Fig. 1 of Gregor et al., the unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) has at least the size of,a region. Furthermore, to withstand common standard thermal stress cycles, the multilayerboard must withstand more than 400 thermal stress cycles per Mil Std 202.Inherently, any multi-layer board withstood the more than 400 thermal stress cyclesper Mil Std 202 which is thermal cycling of assembled circuits between-55 and 125 degrees Celsius with no failures in solder joins. Thus, the unpatterned solid planearea (at the solid and

> non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) of Gregor et al. would withstand the common standard thermal stress cycles.
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> Alternatively, not relying of Gregor et al.'s disclosure that the limitation "the unpattened solid plane area being at least the size of a region in which strain due to thermal cycling from 125°C to -55°C is greater than the strain at which cracking will occur in the absence of the unpatterned solid plane area" is taught by Hanson et al. in e.g., column 4, lines 54 - 65 an entire area of a circuit board withstanding more than strain due to thermal cycling from 125°C to-55°C without cracking or failures. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the area of the circuit board that withstands more than strain due to thermal cycling from 125°C to -55°C without cracking or failures of Hanson et al. into the substrate of Gregor et al. as taught by Hanson et al. to produce an average thermal coefficient of expansion of approximately 8.9 * 10^{6} inch per inch per degree Celsius (column 4, lines 57-60).

Applicants have amended independent claims 1 and 4 to include the limitation that the unpatterned solid plane area extends beyond the corner of the chip attach location for a distance equal to at least two contact pad rows and extends under the corner of the chip attach location for a distance equal to at least one contact pad row. This amendment is supported by the specification, e.g., at p. 14, lines 7-9 and Figs. 13a and 13b.

Applicants respectfully submit that the references cannot support a case of *prima facie* obviousness as to the claims because, among other possible reasons, the cited references do not provide a motivation or suggestion for an unpatterned solid plane area extending beyond the corner of the chip attach location for a distance equal to at least two contact pad rows and extending under the corner of the chip attach location for a distance equal to at least one contact pad row because the invention in Gregor is directed toward a multi-layer interposer in which the X-Y engineering change wiring pattern in the interposer terminates in a pattern of pads on the upper surface of the interposer around the periphery of the chip, and does not address thermal issues, cracking, etc.

Applicants submit that the Examiner's arguments do not meet, particularly with regard to the newly amended claims, the burden of establishing a *prima facie* case of obviousness. As stated in *In re Jones*, 958 F.2d 347 (Fed. Cir. 1992), in order to complete the PTO's *prima facie* case and shift the burden of going forward to applicant, there must be some evidence (other than speculation by the PTO) that one of ordinary skill in the subject art would have been motivated to make the modifications of the prior art necessary to arrive at the claimed subject matter (emphasis added). The recent Supreme Court decision of *KSR Int'l. Co. v. Teleflex, Inc.* does not negate the need for the Examiner to identify the reason why a person of ordinary skill in the art

would have combined the prior art elements in the manner claimed. The fact that the illustration in Gregor shows a solid non-pad area between two solder pads (20) on a board attach surface does not support the Examiner's conclusion that "in a device where a crack does not occur, it can be assumed that the size [of the solid non-pad area on the board attach surface] is greater than the size at which the strain causes a crack [in the chip attach surface], as if it weren't then the crack would occur" because the solid non-pad area is not even mentioned in Gregor nor is common standard thermal stress cycles mentioned. Therefore, the Examiner has provided no factual basis for the conclusions made in the rejection.

Applicants further submit that Hanson teaches a means for addressing cracking problems that is an alternative to the present invention. Specifically, Hanson teaches the use of metal stabilizing layers inside the multi-layer circuit board, not on the board attach surface. *See* Hanson, e.g., at col. 3, lines 33-43. Furthermore, the stabilizing layers of Hanson are not a solid plane, but instead have enlarged apertures filled with epoxy resin. *See* Hanson, e.g., at col. 3, lines 44-48 and col. 4, lines 21-24. Although the Examiner argues that Hanson teaches a solid plane, the specification defines a solid plane as an area of single material having no geometric discontinuities and geometric discontinuities are defined as a feature such as a contact pad or an opening that interrupts a continuous area of material. *See* specification at p. 3, lines 11-12 and 15-16. Therefore, the combination of the teachings of Hanson and Gregor still would not disclose or provide motivation for the present invention.

Furthermore, there could be no reasonable expectation of success because neither references gives any indication that providing an unpatterned solid plane area on the board attach surface surface adjacent to a corner of a chip attach location, wherein the unpatterned solid plane area extends beyond the corner of the chip attach location for a distance equal to at least two contact pad rows and extends under the corner of the chip attach location for a distance equal to at least one contact pad row will inhibit cracking. As mentioned above, Gregor does not mention any relationship between the structure of its interposer and cracking issues and Hanson teaches an alterative solution. At most, any suggested teachings of the prior art references might provide an obvious-to-try situation regarding an unpatterned solid plane area on the board attach surface adjacent to a corner of a chip attach location to prevent cracking on the chip attach surface. As taught in *In re Eli Lily & Co.*, 902 F.2d 943 (Fed. Cir. 1990) an "obvious-to-try" situation exists

when a general disclosure may pique the scientist's curiosity, such that further investigation might be done as a result of the disclosure, but the disclosure itself does not contain a sufficient teaching of how to obtain the desired result or indicate that the claimed result would be obtained if certain directions were pursued. However, nothing in the cited references would even make it obvious to try an unpatterned solid plane area extending beyond the corner of the chip attach location for a distance equal to at least two contact pad rows and extending under the corner of the chip attach location for a distance equal to at least one contact pad row to inhibit cracking.

In addition, these references do not disclose all the elements of the present invention because they do not disclose an unpatterned solid plane area on the board attach surface adjacent to a corner of a chip attach location, wherein the unpatterned solid plane area extends beyond the corner of the chip attach location for a distance equal to at least two contact pad rows and extends under the corner of the chip attach location for a distance equal to at least one contact pad row.

For these reasons, Applicant(s) submit that the cited references will not support a 103(a) rejection of the claims and request that the rejection be withdrawn.

Claims 2, 3 and 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregor et al. and Hanson et al. as applied to claims 1 and 4 above, and further in view of Lau (U.S. Pat. No. 6,075,710).

The Office Action essentially states:

> Regarding claims 2, 3 and 5 - 7, while Gregor et al. and Hanson et al. disclose the use of the dielectric and metal materials on the board attach surface of the substrate, Gregoret al. and Hanson et al. do not disclose a solder mask on the dielectric material (claim 2) and metal (claim 6), the solder mask being a polyimide (claims 3 and 7) and the metal material being copper (claim 5). Lau teaches in e.g., Fig. 4A a solder mask (155 or 235; column 5, lines 65 - 67) on a dielectric material (the dielectric material in the bottom of the substrate; column 5, lines 19 and 20) and metal (Cu 130; column 5, lines 38 - 40) and the solder mask being a polyimide (column 7, line 39. Since the element 235 of Lau works as a mask layer for the solder pastes 245, the element 235 reads as a solder mask. Since the solder mask 235 is made by a polyimide material, Lau discloses a polyimide material for the solder mask). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to m h e r apply the solder mask (e.g., polyimide) of Lau to cover the dielectric material and metal on the unpatterned solid plane area of Gregor et al. and Hanson et al. as taught by Lau to provide finer pitches between the external connections (column 6, lines 4 - 6).
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> Regarding claim 8, Gregor et al., as modified, discloses a solder mask (155 of Lau) having a plurality of openings (the openings for the pads 130 of Lau) defining ballgrid array pads (see e.g., Fig. 3C).

Applicants incorporate by reference their response above to the rejection of claims 1 and 4 as being unpatentable over Gregor in view of Hanson and submit that the addition of Lau does not overcome the deficiencies of Gregor and Hanson as prior art references

For these reasons, Applicant(s) submit that the cited references will not support a 103(a) rejection of the claims and request that the rejection be withdrawn.

In addition to the foregoing arguments, Applicant(s) submit that a dependent claim should be considered allowable when its parent claim is allowed. *In re McCarn*, 101 USPQ 411 (CCPA 1954). Accordingly, provided the independent claims are allowed, all claims depending therefrom should also be allowed.

Based on the foregoing, it is submitted that the application is in condition for allowance. Withdrawal of the rejections under 35 U.S.C. 103 is requested. Examination and reconsideration of the claims are requested. Allowance of the claims at an early date is solicited.

The Examiner is invited to contact Applicant(s)' attorney if the Examiner believes any remaining questions or issues could be resolved.

Respectfully submitted,

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Date

By: Melanie Gover
Melanie G. Gover, Reg. No.: 41,793
Telephone No.: 512-984-4308

Office of Intellectual Property Counsel
3M Innovative Properties Company
Facsimile No.: 651-736-3833